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Failed
Saved
(3324) memory and packag$3 and board and (register with address$3)
(1825) memory and packag$3 and (circuit near3 board) and (register with ad
(24) (memory and packag$3 and (circuit near3 board) and ((register with ad
(155) ((memory near2 module) and pack$4 and (pcb (printed near3 circuit ne
(458) (memory and module and packag$3) and T$OP
(3) ((memory and module and packag$3) and T$OP and gigabyte
(626) (memory and module and packag$3) and gigabyte
(3683) (memory and module and packag$3) and (wide width) and (height high)
(1) (((memory and module and packag$3) and T$OP) and ((memory and module a
(51) (memory and module and packag$3) and (bilateral$2 with symmetr$6)
(27) (memory and module and packag$3) and (bilateral with symmetr$6)
(1) ((memory and module and packag$3) and gigabyte) and ((memory and modu
(76) ((memory and module and packag$3) and T$OP) and ((memory and module a
(145) ((memory and module and packag$3) and gigabyte) and ((memory and mod
(422) memory and packag$3 and (circuit near3 board) and ((register with ad
(312) (memory and packag$3 and (circuit near3 board) and ((register with a
(25562) memory and module and packag$3
(357) (memory and module and packag$3) and (first adj row) and (second adj
(2) (memory and module and packag$3) and (lateral$2 near2 half)
(2) (memory and module and packag$3) and (lateral$2 near2 hal$3)
(4101) memory and module and ((IC chip) with arrang$5)
(894) (memory and module and ((IC chip) with arrang$5)) and ((IC chip) wit
(0) ((memory and module and ((IC chip) with arrang$5)) and ((IC chip) with
(17922) 711/$.ccls.
(4521) 711/$.ccls. and module
(1369) (711/$.ccls. and module) and row

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Default operator | DR

☒ Highlights all hit names in bold

[illegible]

 ORS form
  B4R form
  Image
  Text
  HTML

[illegible]